

SILICON SHEET FROM SILANE: FIRST RESULTS

C. Rodrigues Pinto^{*}, R.C. Gamboa, J.C. Henriques, J.M. Serra, J. Maia Alves and A.M. Vallera

Physics Department/CCMM, University of Lisbon,
Campo Grande, P-1749-016 Lisboa, Portugal

Abstract

A process to obtain self-supported thin silicon films is being developed. Films are grown by optical CVD (using halogen lamps as heating system) from silane, at low temperature and relatively high growth rates, on silicon substrates with a sacrificial layer of porous-Si, which allows film detachment. The porous silicon layer was formed by anodization of the Si-substrate surface in a HF:ethanol solution.

Film deposition was carried out in an optical cold wall horizontal CVD reactor, operating at atmospheric pressure, and specially designed for this study. Deposition rates and film morphology were studied as a function of substrate nominal temperature, gas concentration and flux. In the final chosen conditions, deposition occurs at a nominal temperature of 840C, with a silicon growth rate between 2 and 4 $\mu\text{m}/\text{min}$, which is relative high for the low temperature used. A good usage of silane gas was already achieved, with 80 to 85% of the silicon in the silane gas being deposited on a 40x40mm² substrate, with very low deposition rate on the reactor wall. Films of thicknesses from 10 to 150 μm were deposited. The films were found to be continuous, with surfaces coated with whiskers.

Film detachment from multicrystalline substrates has proved unsuccessful so far, while it readily occurs when monocrystalline substrates are used. The reason for this is macropore collapse and film rupture usually occurring in the smaller grain regions of the multicrystalline substrates.

Keywords: Silicon, CVD, Silane, Porous- Si

1. Introduction

The production of silicon sheet directly from silane (or chlorosilanes) is an interesting proposal for photovoltaic cell fabrication, since it bypasses expensive, energy and material wasting steps. One obvious problem is that some substrate is needed onto which silicon can be deposited by chemical

vapour deposition (CVD); the deposited silicon film can then either be left adhering to the substrate, or be detached from it.

One approach to detachable silicon film that has raised much interest in recent years [1][2] [7] uses monocrystalline silicon wafers as the substrate, with the advantages of no contamination nor thermal stress induced by different thermal expansion coefficients. Detachment is carried out through an elegant procedure: a sacrificial layer of porous silicon (PS) is electrochemically formed on the surface of the wafer. Since PS retains the crystal orientation of the underlying material, epitaxial CVD produces a single crystalline film with the same orientation as that of the substrate; and the porous layer can be made sufficiently weak to allow detachment. Thin monocrystalline silicon sheet can thus be produced at potentially reasonable cost, the original high cost of the substrate being divided by its successive re-utilisations.

Here we report our first results on the study of an alternative approach to the production of detachable silicon sheet. In our approach (figure 1), we aim at low temperature, ambient pressure CVD deposition of polycrystalline silicon on a low cost substrate using silane as the feedstock gas. Good crystalline quality is achieved in a separate step, consisting of zone melting of the detached film. Low temperature deposition allows interesting possibilities for low cost detachable substrates, which are being considered. In the present work, however, it was our aim to concentrate on the study of the CVD step, and so decided to use for the moment, for film detachment, the by now reasonably well known porous layer technique.

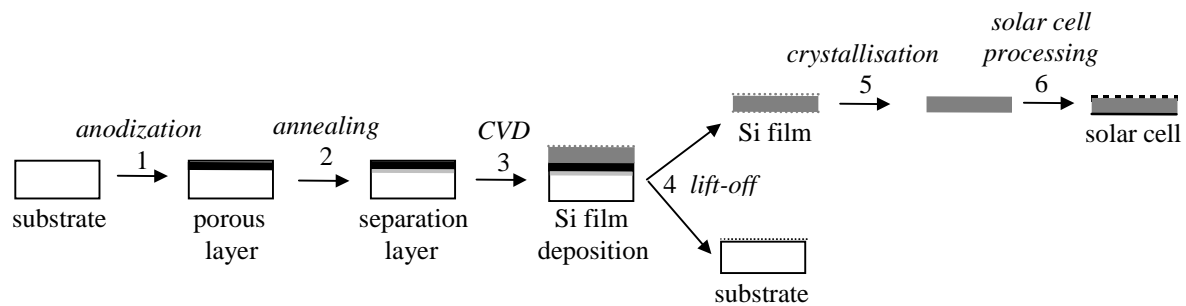


Figure 1 - Schematic description of the conceived process under study. The present work concentrated on the CVD step.

2. Substrate preparation

Substrates used in this study were mainly p-type multicrystalline silicon wafers 330 μ m thick with 0.5-2 Ω .cm, cut to 40x40 mm² area, polished and cleaned by usual chemical processes prior to any further preparation. A few single crystalline Czochralski wafers, similarly prepared, were also used, when problems arose with film detachment from the multicrystalline substrates, in order to confirm the origin of the problems encountered.

The porous silicon layers were obtained by anodic corrosion in the electrochemical reactor schematically represented in Figure 2.

Following [1], we used a three step process to produce the porous silicon layer: after an initial low current density and an intermediate current density, a final high current density is applied. The two first steps are intended to form a low porosity superficial layer. The third step forms a deep high porosity layer that should act as the separation layer.

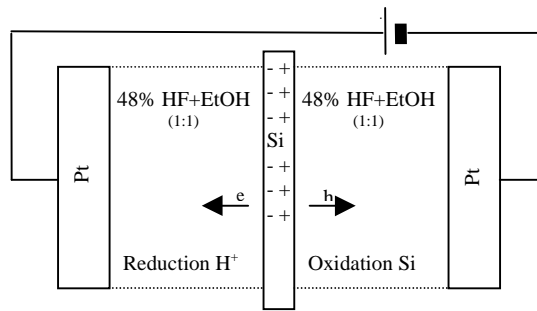


Figure 2 - Schematic representation of the electrochemical reactor used in this work. Silicon substrates are placed between the two chambers containing 48% HF:EtOH solution (1:1). The electric contacts are two platinum plates on each side of the reactor. The tubes on top ensure electrolyte renovation during anodisation, which was found to be important for uniform corrosion.

A study of anodic corrosion conditions was carried out which included measurements of porous layer rate growth, of layer porosity and of electronic charges per removed silicon atom. Porosity was calculated using a gravimetric method (lost mass after anodisation) and the thickness of the porous layer as measured on scanning electron microscope (SEM) images. The results shown in Table 1 were obtained from measurements in about 25 samples per current density studied, which showed remarkable reproducibility. No noticeable differences in layer thicknesses were observed for different crystal grains.

Table 1
PS layer thickness rate, mass loss rate, electrical charge per removed silicon atom and porosity for anodic corrosion at different current densities.

current density (mA/cm ²)	corrosion rate		electron/ /Si atom	porosity (%)
	µm/min	mg/min		
5	0.60	0.46	1.91	35-40
10	0.90	0.91	1.92	44-50
100	5.31	7.80	2.25	63-69

Porous silicon changes its structure when annealed at high temperature (>800°C) in hydrogen. This is particularly noticeable in the high porosity layer, as shown in figure 3: reduction of the excess surface free energy leads to large cavities, or macropores, with dimensions of the order of 1µm, and several mechanically fragile columns. The high porosity layer is thus turned into a separation layer. Most of the samples used as substrates for CVD were annealed at 1100°C in hydrogen for 45 minutes. A few were not annealed at all, while others were annealed only following the CVD step, but these alternatives proved less successful than this standard treatment, if anything.

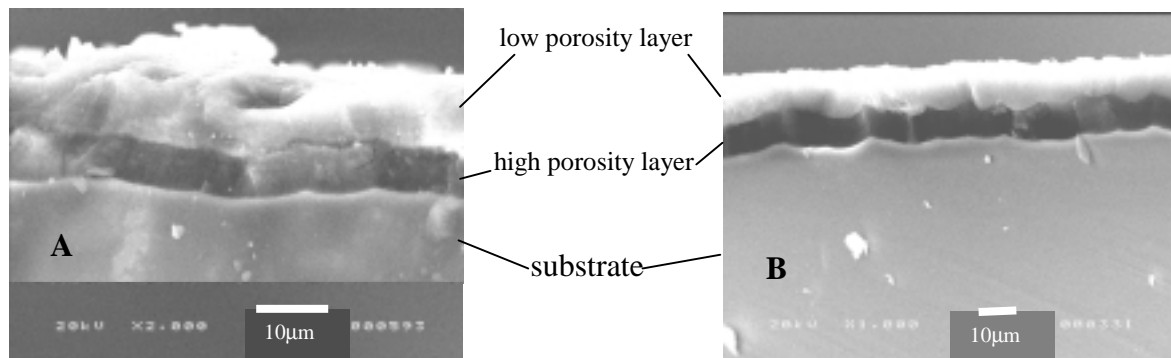


Figure 3 - Demonstration of the re-organisation of the porous layer by high temperature annealing. A: substrate with porous layer before annealing; B: the same substrate after annealing at 1100°C in hydrogen during 45 minutes. Notice the well defined voids and columns that develop after the annealing step. Notice also the good thickness uniformity and definition of the porous layers.

3. Polycrystalline Silicon film Growth by CVD from silane

The aim was to search for atmospheric pressure CVD conditions such that a continuous detachable film (appropriate for further processing) would be obtained at a growth rate as high as possible, while keeping (i) temperature as low as possible, (ii) negligible deposition rate on furnace walls, (iii) yield (defined as the mass of deposited silicon film per mass of silicon in feedstock gas) as high as possible. The chosen strategy was to use a cold wall optical furnace specially conceived for this study, and to explore a range of temperatures (400 to 950°C), of gas compositions (silane and HCl concentrations from 2 to 10% in hydrogen) and gas fluxes (from 0.3 to 3 l/min), of substrate treatments and of heating element geometries.

A satisfactory compromise was reached, with a deposition rate of 2 to 4 µm/min at a nominal temperature of only 840°C, as described in Table 2. At higher temperatures and silane concentrations, deposition on the walls occurred, such as shown in figure 4. This figure is interesting in that it shows that a very well defined convection flow pattern sets in, its quasi symmetry indicating that longitudinal gas flux velocity is negligible compared with convection driven currents. This helps to explain the very high yields already reached, with 80 to 85% of the silicon mass in feedstock gas being deposited on a mere 40×40 mm² substrate. The conditions found are, of course, expected to be furnace and substrate dependent to some extent, but nevertheless constitute a definite demonstration that a good compromise is possible.

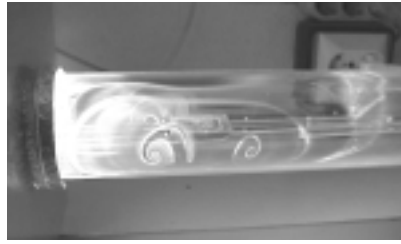


Figure 4 - Furnace tube after a high temperature, high silane flux deposition experiment, clearly showing deposition on the walls denouncing a definite convection pattern.

In order to determine whether deposition rates were being altered as the film started to grow, either due to changes in the optical and chemical properties of the substrate surface or to furnace conditions, several batches of samples with different deposition times were produced. One such experiment for the described growth conditions is shown in figure 5, demonstrating that the deposition rate is quite independent of time.

Table 2
Present conditions for silicon film growth

Nominal temperature	840°C
Gas composition	3.3% SiH ₄ + 0% HCl in H ₂
Gas flux	0.3 l/min
Film thickness	10 to 300µm
Deposition rate	2 to 4 µm/min
Si mass conversion efficiency	80 to 85 %
Deposition rate on reactor walls	Negligible

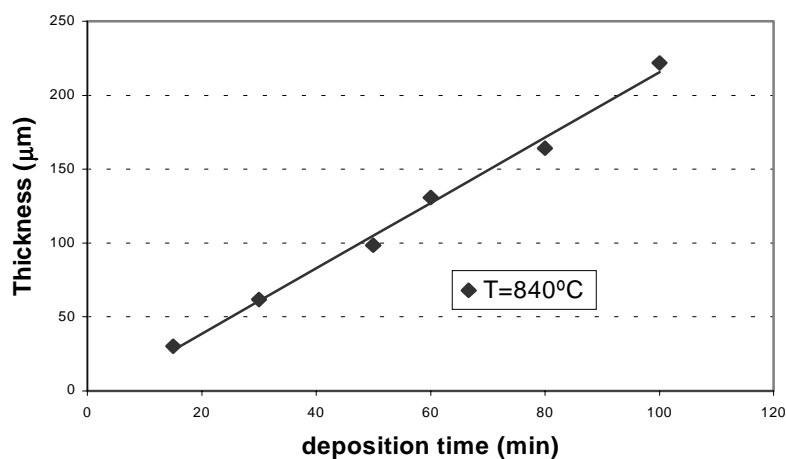


Figure 5. Thickness of deposited silicon film (measured gravimetrically) versus deposition time. A constant growth rate of 2.22µm/min is observed. CVD conditions were as in Table 2.

The deposited films are formed by a continuous region (including some voids) covered by different types of superficial growth structures. While, in our present growth conditions, the deposition rate is only slightly dependent on the existence of the porous layer, surface morphology does reflect its existence or absence. Figure 6 demonstrates clearly that the film grown on the porous layer (top) is only slightly less thick than that grown on the lower untreated substrate surface; however, the whisker structures that cover the film surfaces are definitely thinner and more intricate on the porous silicon side than on the non-porous side. Such rough surfaces present no problem, since all these structures will be molten and incorporated during the crystallisation step.

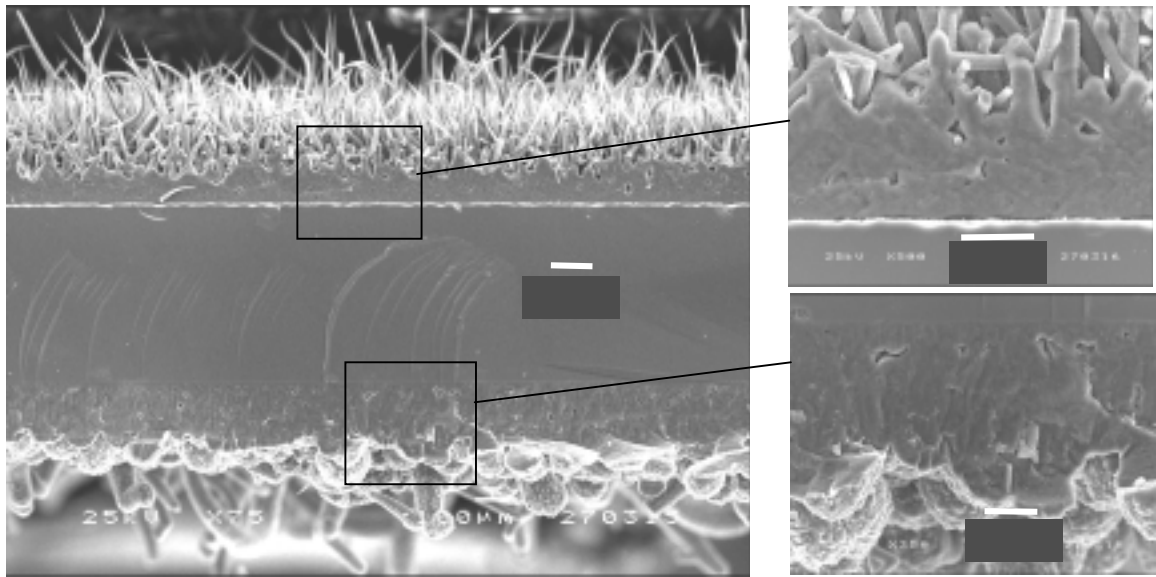


Figure 6 - CVD on porous (A) and untreated (B) substrate surfaces. The substrate had a porous layer on the upper surface, but no treatment on the lower surface. Total silicon mass deposited on each side is only slightly different, but surface morphologies of the deposited films differ noticeably. Growth conditions were as in Table 2.

4. Film detachment

Film detachment proved impossible in all our samples using multicrystalline substrates. Since we had closely followed other author's prescriptions, and explored parameter variation around these, and all observations and measurements of the PS layer seemed to point towards ease of detachment, this came as a surprise. We decided to try detachment in a few Czochralski monocrystalline substrates, and this was met with immediate success. A study of the porous separation layer was then carried out to try and understand the reasons for this different behaviour, and we were finally led to the following conclusion:

Although the as grown PS layer seemed almost as uniform in multicrystalline substrates as in single crystals, after annealing at high temperature the multicrystalline samples always showed defects that apparently could be classified into two types, macropore collapse and rupture of the upper PS layer, as demonstrated in figures 7 to 9. These defects seemed to occur always in regions of small grain size; so far, no such defects were observed in large grains.

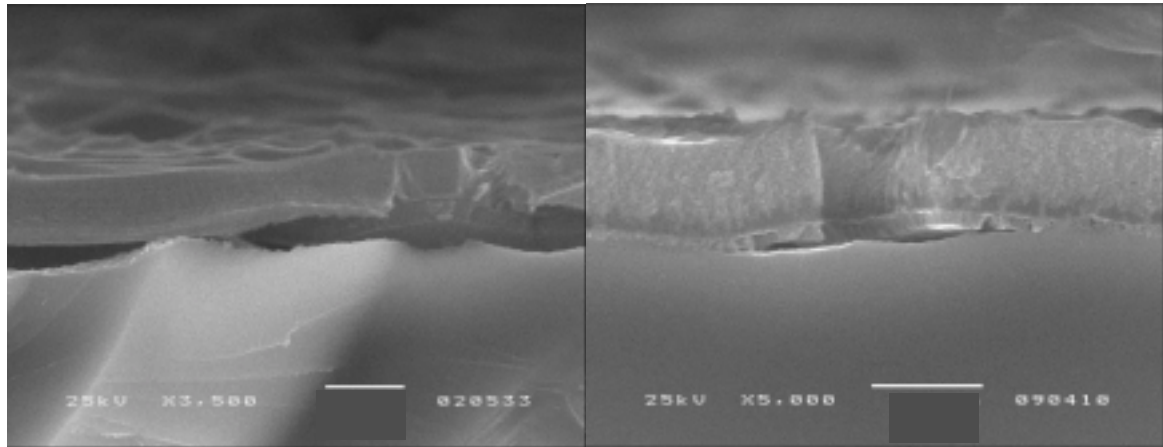


Figure 7 - Defects in the separation layers after the annealing step: macropore collapse (A) and upper PS film rupture (B).

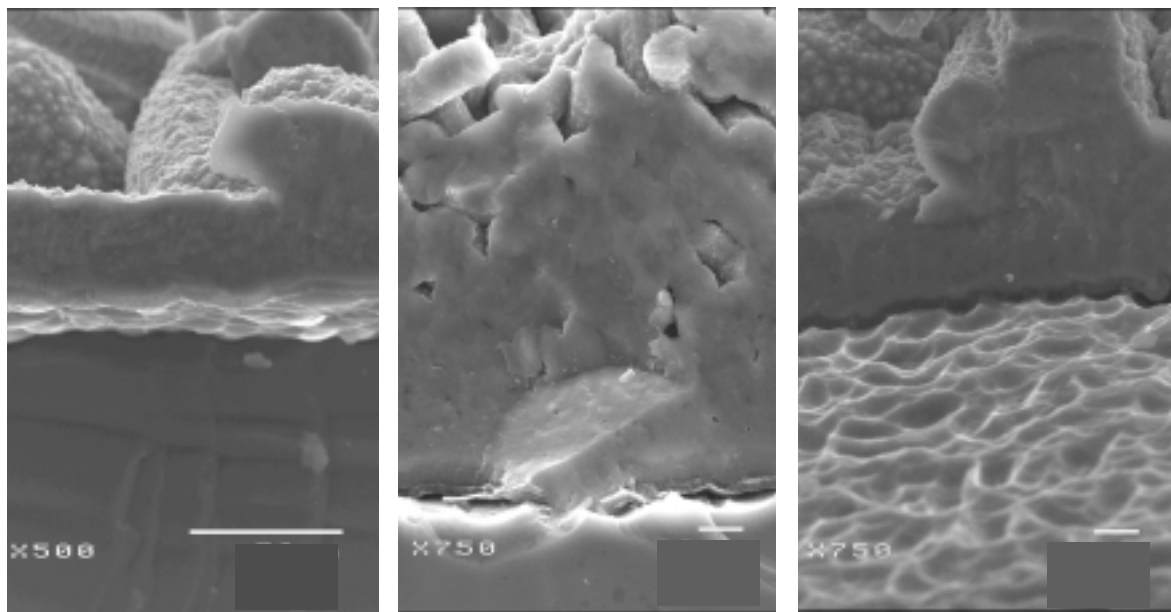


Figure 8 - Separation layers after annealing and film deposition in monocrystalline (A), small grain multicrystalline (B) and large grain multicrystalline (C). Notice the uniformity of the separation layer in cases A and C, and the solid bridges in B that make detachment impossible.

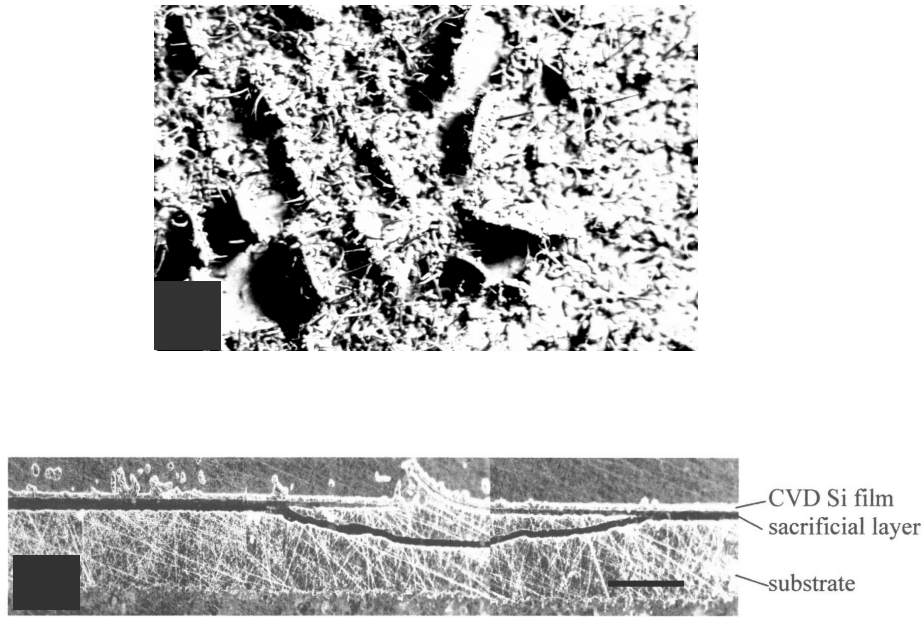


Figure 9 – A: Sample displaying severe peeling of PS layer, with silicon film being deposited under the separation layer; B: cross section of such a sample, showing the problems caused by peeled PS film: film detachment occurs in the rest of the sample, but the solid bridge at the defect is sufficiently strong to cause substrate breakage when detachment is forced.

5. Film crystallisation

Due to the problems with film detachment, the crystallisation step was not yet tried in detached films. Molten zone crystallisation was carried out only in a few undetached samples, consisting of a 300 μm thick multicrystalline Si substrate with grown films (100 μm thick) on either side, in order to check for contamination. The overall thickness was in the order of 500 μm . Minority carrier diffusion lengths were measured in these crystallised samples by the Surface Photo-Voltage technique. The result was an average of about 90 μm , which is a usual value when crystallising good uncontaminated material (without bias light, and before gettering or defect passivation). The conclusion is that no contamination attributable to our process steps was detected.

6. Conclusions

The study of an alternative process for detachable silicon film was initiated. Conditions for satisfactory deposition of silicon film by atmospheric pressure CVD from silane were found: deposition rates of 2 to 4 $\mu\text{m}/\text{min}$ were demonstrated at a low substrate temperature (840C), with high silicon mass yield (80 to 85% of silicon mass in silane was deposited in 40 \times 40mm² substrates) and negligible deposition on furnace walls.

The present strategy for film detachment, based on a porous silicon sacrificial layer, met unexpected difficulties when applied to multicrystalline substrates. This is due to solid bridge formation associated with defects in the porous silicon layer, which arise during the high temperature annealing step.

Acknowledgements

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References

- [1] Hiroshi Tayanaka, Kazushi Yamanauchi, Takeshi Matsushita, *Thin-Films Crystalline Silicon Solar Cells Obtained by Separation of a Porous Silicon Sacrificial Layer*, Proc. of 2nd World Conference on Photovoltaic Energy Conversion, Viena, Austria, 1998.
- [2] R. R. Bilyalov, C.S. Solanki, J. Poortmans, J. Nijs, *Thin Silicon Films for Solar Cells Based on Porous Silicon*, Proc. of 16th European Photovoltaic Solar Energy Conference, Glasgow, 2000.
- [3] R. L. Smith, S. D. Collins, *Porous Silicon Formation Mechanisms*, Journal Applied Physics, vol. 71, n. 8, 1992.
- [4] L. Stalmans, W. Laureys, K. Said, E. Vazsonyi, M. Caymax, J. Poortmans, J. Nijs, R. Mertens, *The Use of Porous Silicon in Photovoltaic Applications*, Proc. of 14th European Photovoltaic Solar Energy Conference, Barcelona, 1997.
- [5] P. Menna, G. Di Francia, V. La Ferrara, *Porous Silicon in Solar Cells: a review and a description of its application as an AR coating*, Solar Energy Materials and Solar Cells, 37, 1995, pp13-24.
- [6] S. Lazarouk, P. Jaguiro, S. Katsouba, G. Maiello, S. La Monica, G. Masini, E. Proverbio, A Ferrari, *Visual Determination of Thickness and Porosity of Porous Silicon Layers*, Thin Solid Films, 297, 1997, pp 97-101.
- [7] Titus J. Rinke, Ralf B. Bergmann, Jürgen H. Werner, *Efficient Thin Film Solar Cells by Transfer of Monocrystalline Si Layers*, Proc. of 16th European Photovoltaic Solar Energy Conference, Glasgow, 2000.
- [8] J. Bloem, L.J. Giling, *Mechanisms of the Chemical Vapour Deposition of Silicon* in Current Topics in Material Science, Volume 1, ed. Kaldis North-Holland Publishing Company, 1987, Chapter 4.
- [9] Kenneth E. Bean *Chemical Vapour Deposition of Silicon and Its Compounds*, Texas Instruments Incorporated, Dallas, Texas, Chapter 3 in Gary E. McGuire *Semiconductor Materials and Process Technology Handbook*, Microelectronics Centre of North Carolina Research Triangle Park, North Carolina.

